TC40H365P/F
TC40H366P/F

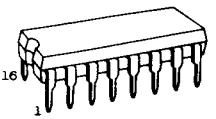
C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40H365 HEX BUS BUFFER NONINVERTED 3-STATE OUTPUT
TC40H366 HEX BUS BUFFER INVERTED 3-STATE OUTPUT

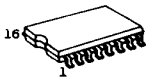
The TC40H365 and the TC40H366 hex bus buffers having 3-state outputs.

High impedance is given to the outputs by setting ENABLE input terminal $\overline{G}_1$ or $\overline{G}_2$ to "H" level.

Further, each output current is large, permitting direct drive of ten LSTTL input lines.



DIP16 (3D16A-P)



MFP16 (F16GC-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	TATING	UNIT
Supply Voltage	V_{DD}	V_{SS}-0.5 ∿ V_{SS}+10	V
Input Voltage	V_{IN}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ∿ V_{DD}+0.5	V
Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300(DIP)/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ∿ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

TRUTH TABLE (TC40H365)

INPUTS			OUTPUTS
ENABLE $\overline{G}_1$	ENABLE $\overline{G}_2$	DATA An	Yn
L	L	L	L
L	L	H	H
H	✱	✱	High Impedance
✱	H	✱	High Impedance

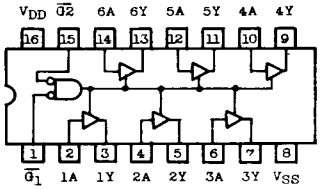
TRUTH TABLE (TC40H366)

INPUTS			OUTPUTS
ENABLE $\overline{G}_1$	ENABLE $\overline{G}_2$	DATA An	Yn
L	L	L	H
L	L	H	L
H	✱	✱	High Impedance
✱	H	✱	High Impedance

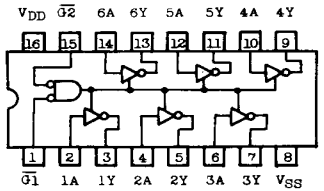
✱ = Don't Care

PIN CONNECTION

TC40H365



TC40H366



RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}	-	2.0	-	8.0	V
Input Voltage	V_{IN}	-	0	-	V_{DD}	V
Operating Temperature	T_{opr}	-	-40	-	85	°C

ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High Level Output Voltage		V_{OH}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	4.95	-	4.95	5.0	-	4.95	-	V
Low Level Output Voltage		V_{OL}	$\|I_{OUT}\|$<1μA V_{IN}=V_{SS},V_{DD}	5	-	0.05	-	0.0	0.05	-	0.05	V
High Level Output Current		I_{OH}	V_{OH}=4.6V V_{IN}=V_{SS},V_{DD}	5	-0.95	-	-0.88	-	-	-0.8	-	mA
Low Level Output Current		I_{OL}	V_{OL}=0.4V V_{IN}=V_{SS},V_{DD}	5	4.7	-	4.4	-	-	4.0	-	mA
Input Voltage	"H" Level	V_{IH}	$\|I_{OUT}\|$<1μA V_{OH}=4.5V V_{OL}=0.5V	5	4.0	-	4.0	-	-	4.0	-	V
	"L" Level	V_{IL}		5	-	1.0	-	-	1.0	-	1.0	V
Input Current	"H" Level	I_{IH}	V_{IH}=8.0V	8	-	0.3	-	10^{-5}	0.3	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0.0V	8	-	-0.3	-	-10^{-5}	-0.3	-	-1.0	μA
Disable Output Current	High Level	I_{DH}	V_{DH}=8.0V	8	-	0.5	-	10^{-4}	0.5	-	5	μA
	Low Level	I_{DL}	V_{DL}=0.0V	8	-	-0.5	-	-10^{-4}	-0.5	-	-5	μA
Quiescent Supply Current		I_{DD}	*V_{IN}=V_{SS},V_{DD}	5	-	5.0	-	0.005	5.0	-	25	μA

* All valid input combinations.

SWITCHING CHARACTERISTICS (Ta=25°C, V_{SS}=0V, V_{DD}=5V, C_L=50pF, R_L=1kΩ)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Rise Time		t_{or}		-	17	35	ns
Outpue Fall Time		t_{of}		-	14	30	ns
High Level Propagation Delay Time		t_{pLH}	Fig.1	-	22	33	ns
Low Level Propagarion Delay Time		t_{pHL}		-	26	39	ns
Output Disable Time	High Level	t_{pHZ}	Fig.2, Fig.3	-	40	50	ns
	Low Level	t_{pLZ}		-	28	42	ns
Output Enable Time	High Level	t_{pZH}	Fig.2, Fig.3	-	37	56	ns
	Low Level	t_{pZL}		-	30	45	ns
Input Capacitance		C_{IN}		-	5	-	pF
Output Capacitance		C_{OUT}		-	16	-	pF

TC40H365P/F
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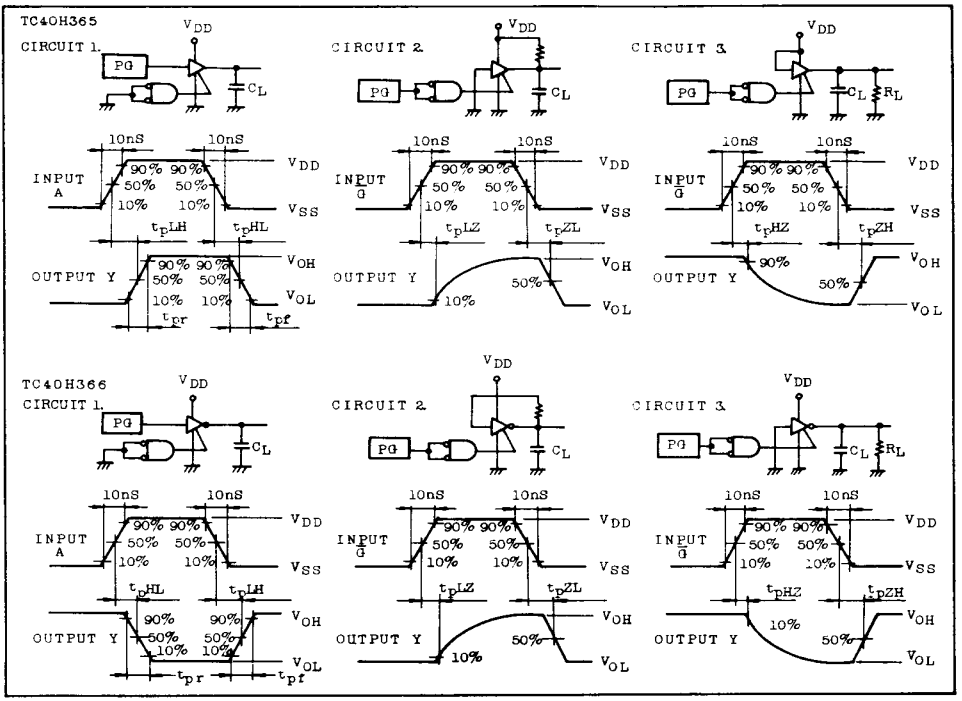
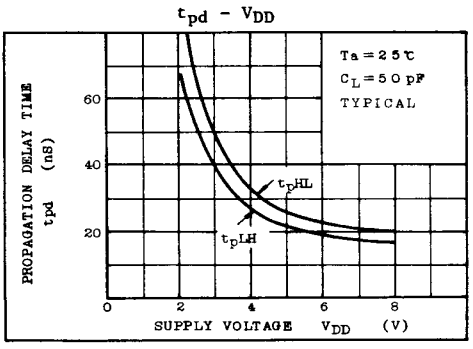
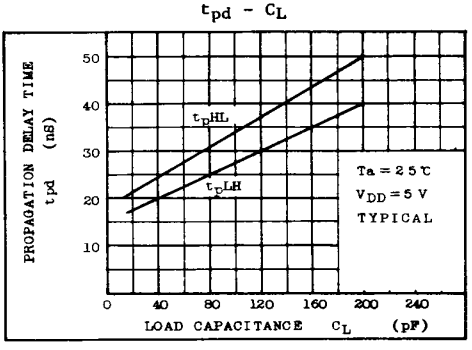
SWITCHING TIME TEST CIRCUIT AND WAVEFORM







TC40H365P/F
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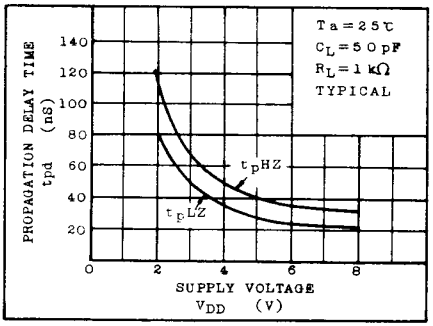
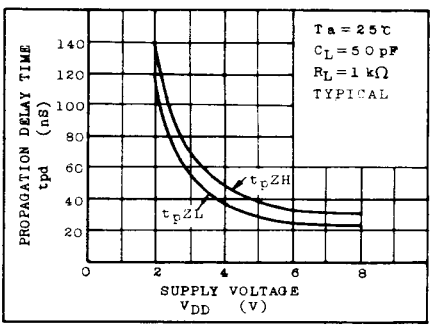
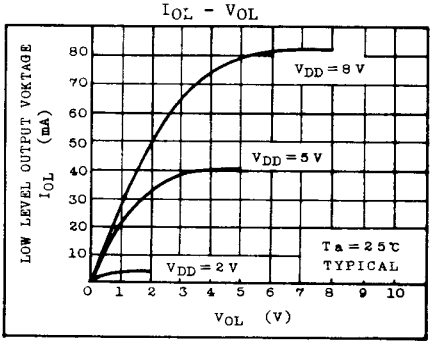
t_{pd} - V_{DD}



t_{pd} - V_{DD}



I_{OL} - V_{OL}



I_{OH} - (V_{DD} - V_{OH})